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# K8T890A01

Version 1.0

VIA K8T890 CF + VT8237/ R / R Plus Chipset  
AMD AM2 Processor

## CPU:

**AMD AM2**

## System Chipset:

**VIA K8T890 CF (North Bridge)**  
**VIA VT8237 / R / R Plus (South Bridge)**

## On Board Chipset:

**BIOS -- LPC EEPROM**  
**Audio Codec -- AC97 ALC653**  
**LPC Super I/O -- IT8716 CX/DX**  
**LAN --PCI LAN (10/100M) RTL8100C / PCI LAN (Giga) 8110SC**  
**CLOCK --ICS 953201 BF**

## Main Memory:

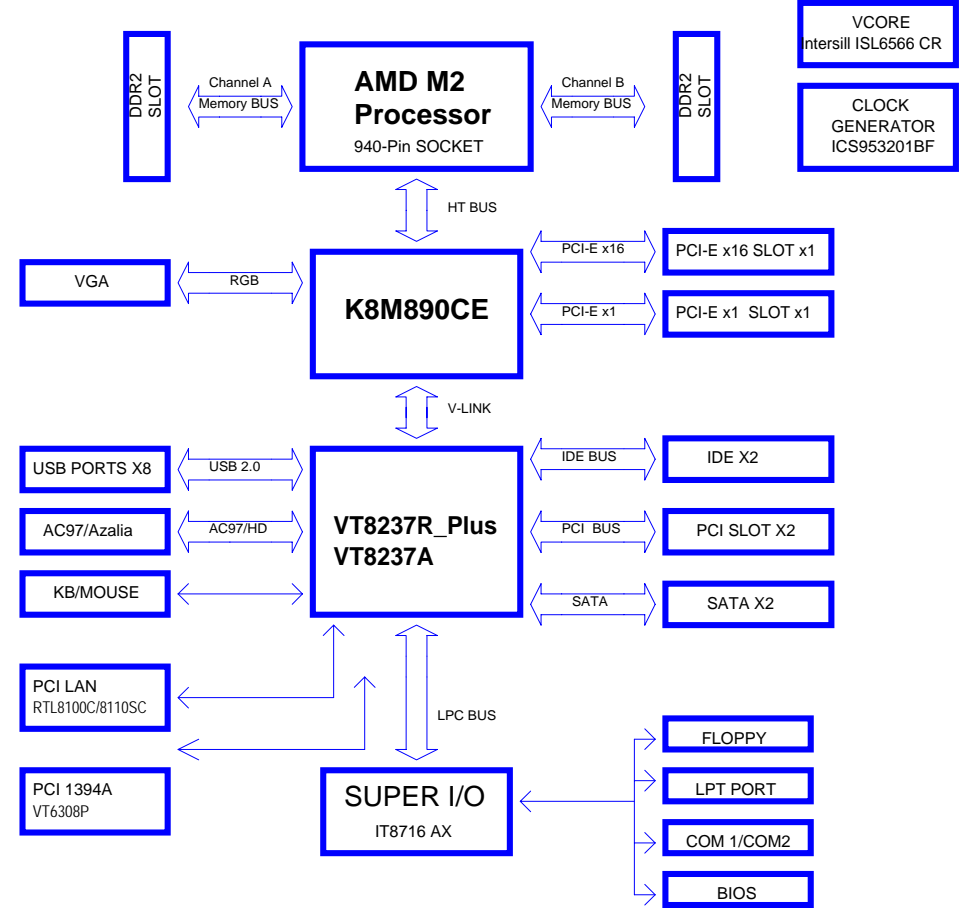
**Dual Channel DDRII DIMM \* 2**

## Expansion Slots:

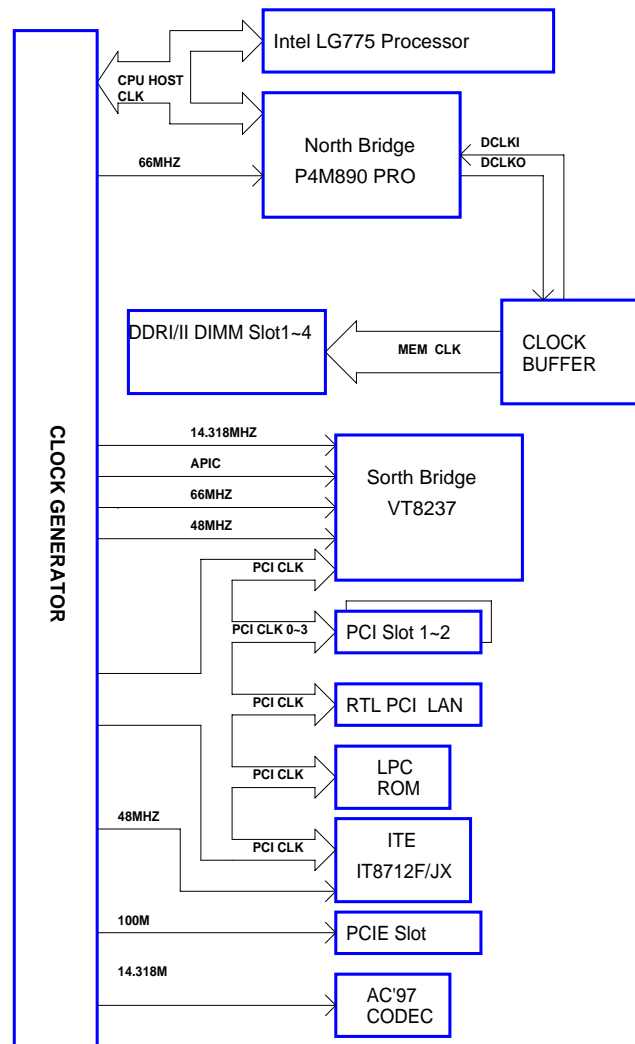
**PCIe 16X SLOT \* 1**  
**PCIe 1X SLOT \* 2**  
**PCI SLOT \*3**

## VRM:

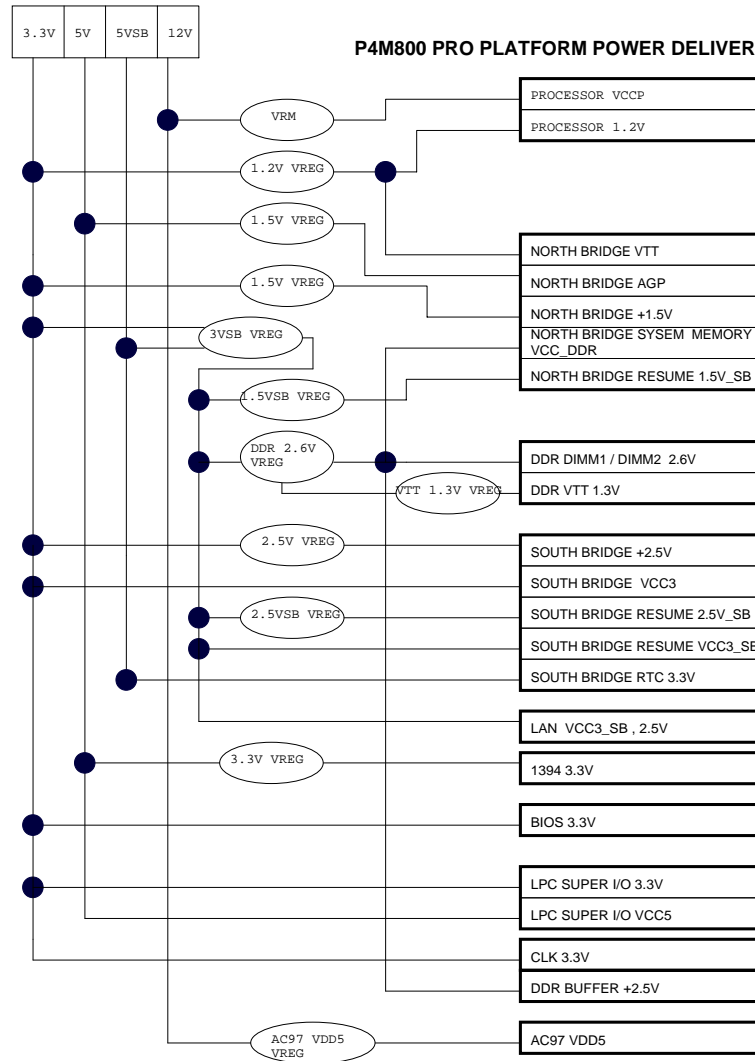
**Controller: Intersill ISL6566 CR**



P4M800 PRO PLATFORM CLOCK GENERATOR MAP



P4M800 PRO PLATFORM POWER DELIVERY MAP



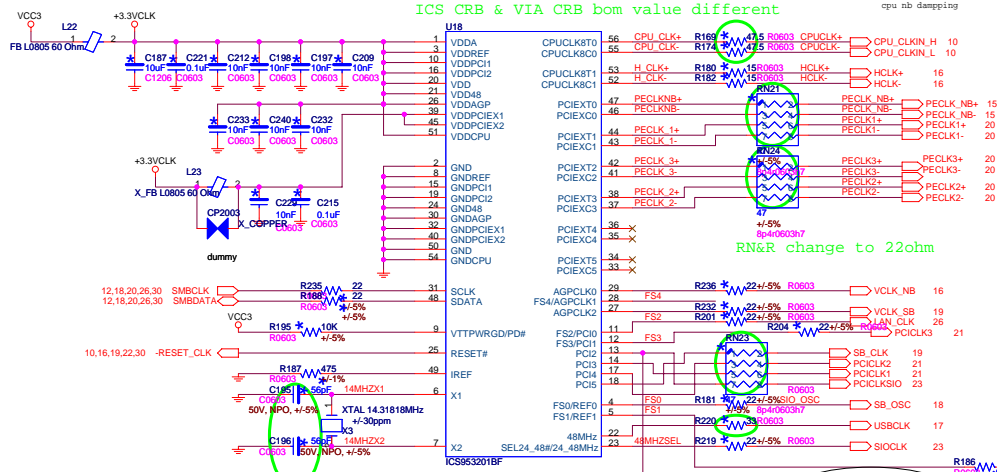
FOXCONN PCEG

Super I/O

[illegible]

# Clock Synthesizer

Delete RN26 , RN27



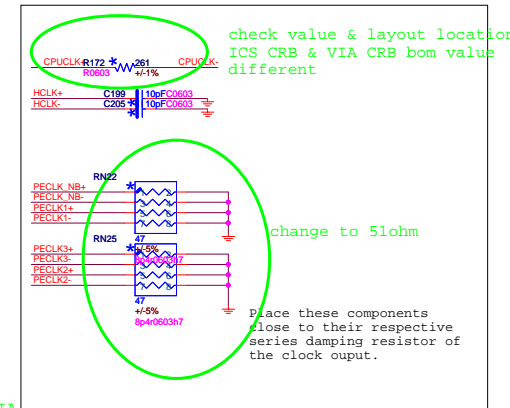
ICS CRB & VIA CRB bom value different

TABLE 拾捌

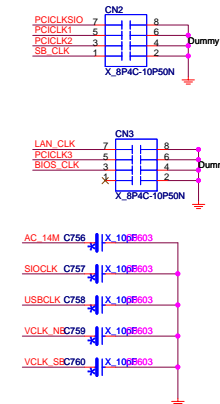
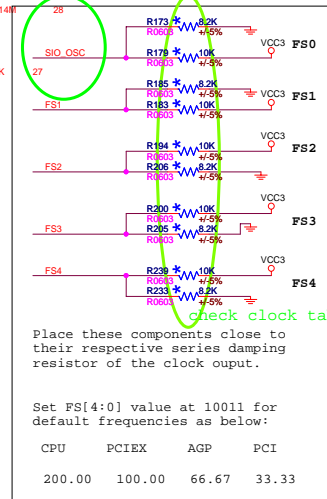
FS[4:0]	CPU	PCIEX	AGP	PCI
00000	100.90	100.90	67.27	33.63
00001	133.90	100.43	66.95	33.48
00010	168.00	100.80	67.20	33.60
00011	202.00	101.00	67.33	33.67
00100	100.20	100.20	66.80	33.40
00101	133.50	100.13	66.75	33.38
00110	166.70	100.02	66.68	33.34
00111	200.40	100.20	66.80	33.40
01000	160.00	100.00	66.67	33.33
01001	202.00	101.00	67.33	33.67
01010	210.00	105.00	70.00	35.00
01011	212.00	106.00	70.67	35.33
01100	270.00	101.25	67.50	33.75
01101	225.00	112.50	75.00	37.50
01110	266.67	100.00	66.67	33.33
01111	300.00	112.50	75.00	37.50

FS[4:0]	CPU	PCIEX	AGP	PCI
10000	100.00	100.00	66.67	33.33
10001	133.00	100.00	66.67	33.33
10010	166.66	104.16	69.44	34.72
10011	200.00	100.00	66.67	33.33
10100	103.00	103.00	68.67	34.33
10101	137.33	103.00	68.66	34.33
10110	171.66	103.00	68.66	34.33
10111	206.00	103.00	68.67	34.33
11000	208.00	104.00	69.33	34.67
11001	210.00	105.00	70.00	35.00
11010	215.00	107.50	71.67	35.83
11011	220.00	110.00	73.33	36.67
11100	226.00	113.00	75.33	37.67
11101	230.00	115.00	76.67	38.33
11110	240.00	120.00	80.00	40.00
11111	250.00	125.00	83.33	41.67

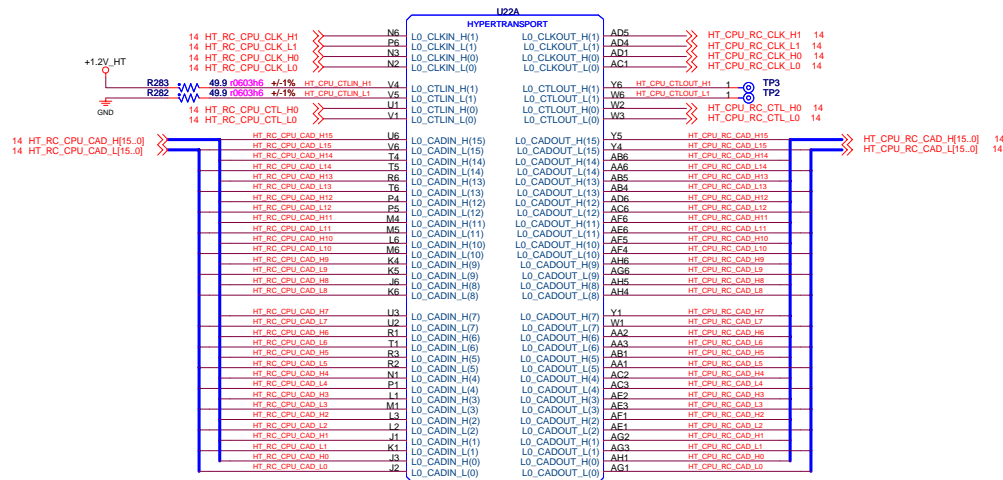
1崩2惠单



CHECK VIA ICS CRB & VIA CRB bom value different



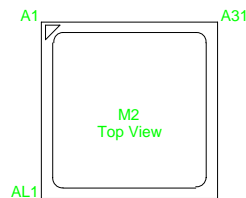


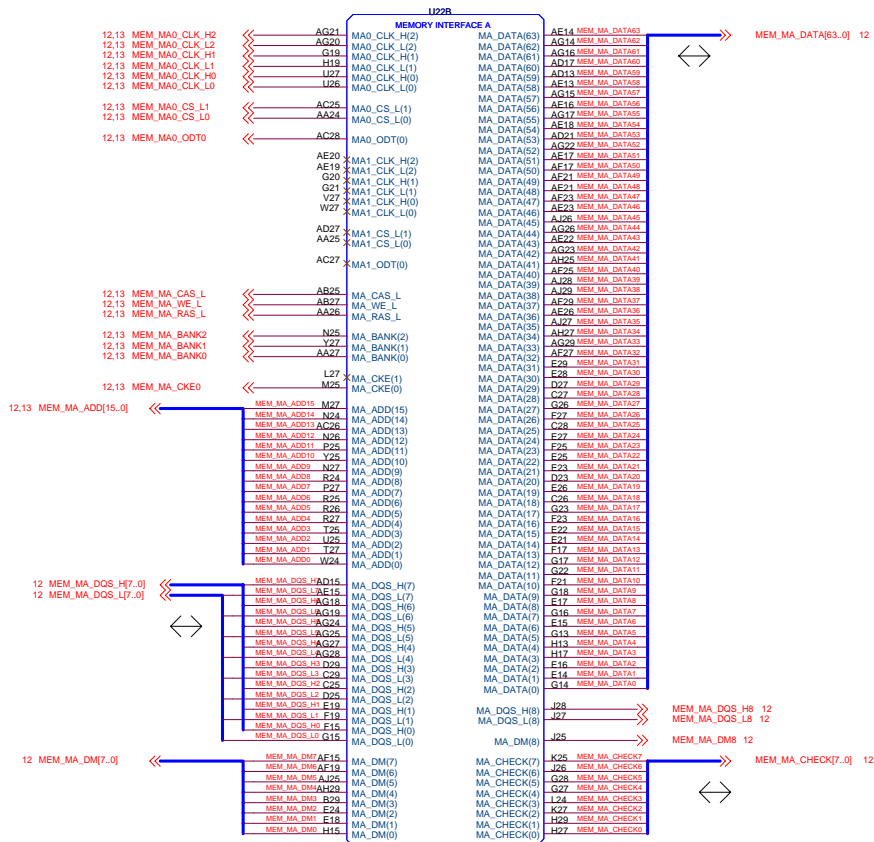


Layout: Add stitching caps if crossing plane split

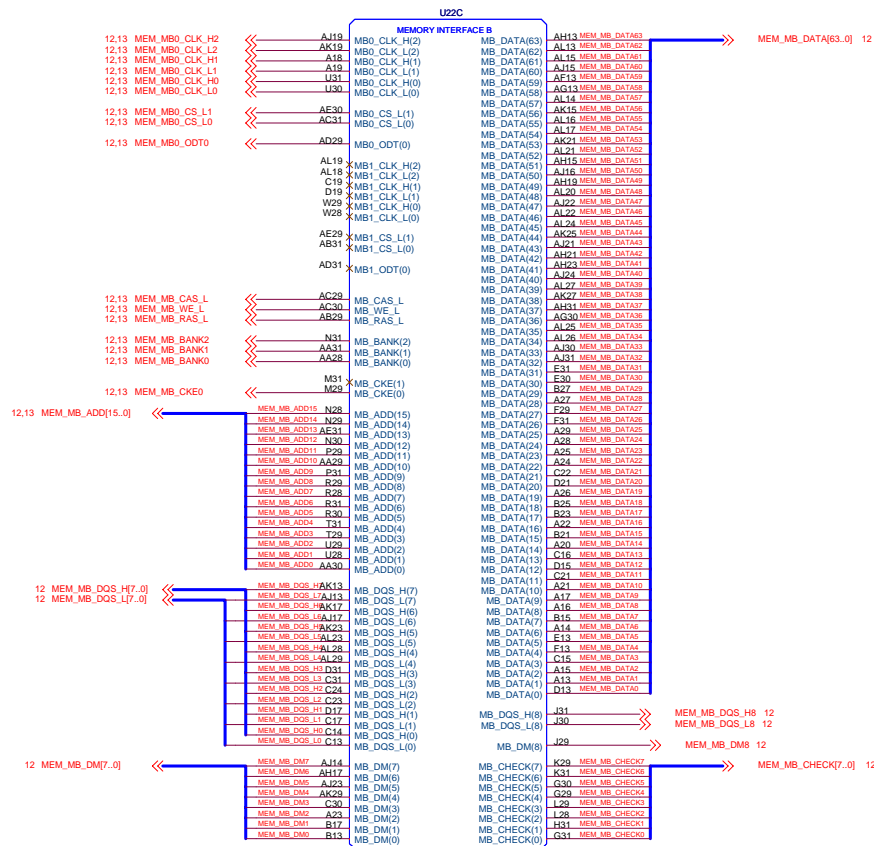
HyperTransport Net Naming Convention

HT\_"link driver"\_"link receiver"\_"function"\_"polarity"\_"number"



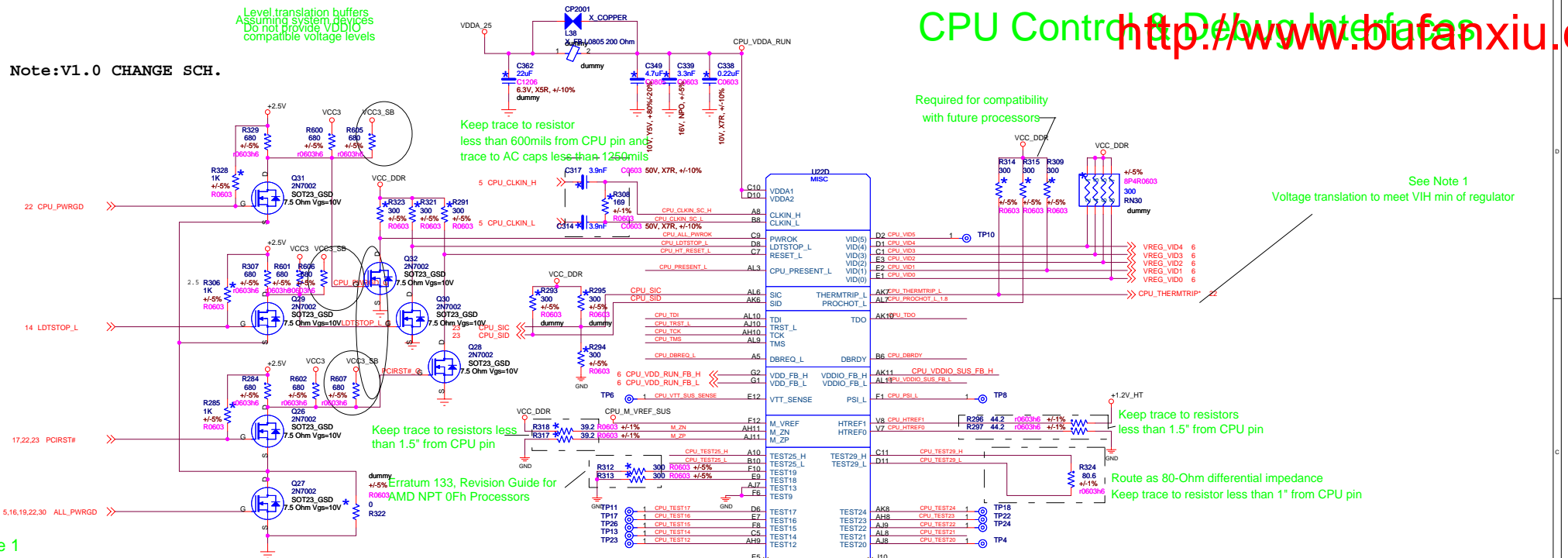






Note:V1.0 CHANGE SCH.

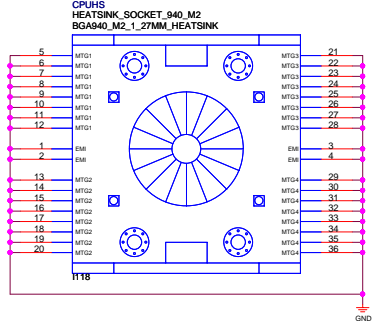
Level translation buffers  
Assuming system devices  
Do not provide VDDIO  
compatible voltage levels



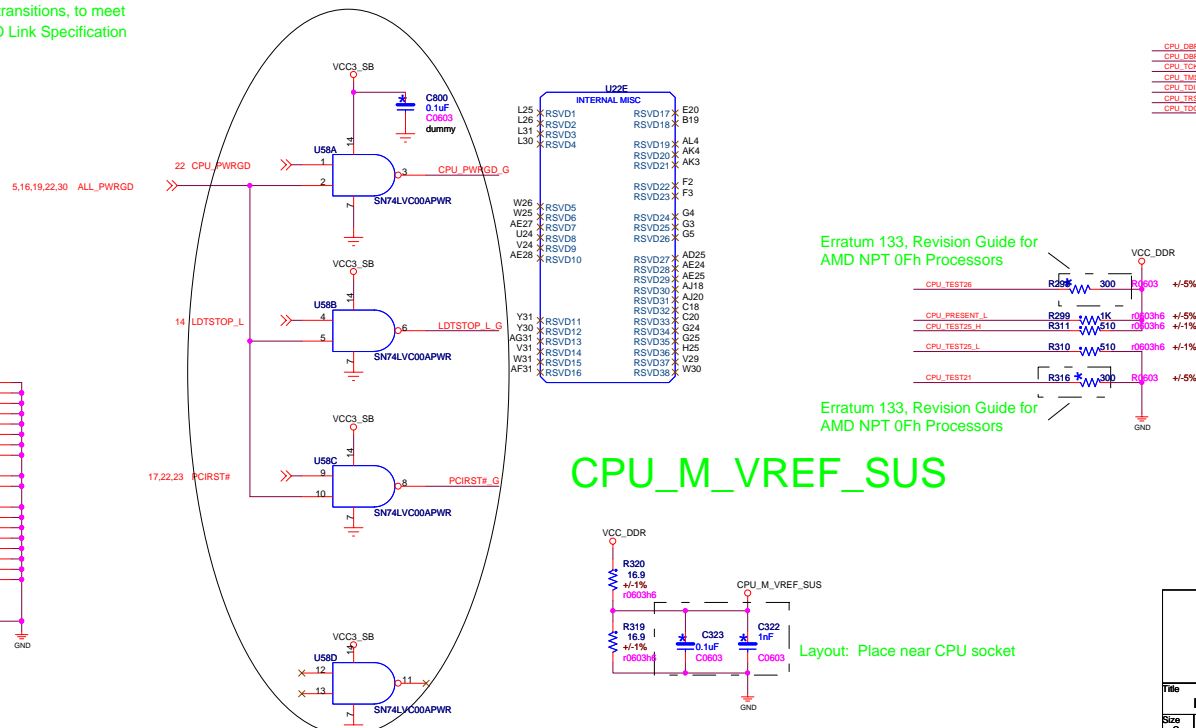
### Note 1

5-bit VID Implementation:  
 VID4:0 connects to VID4:0 of regulator\*  
 VID5 should be left unconnected.  
 VID1 should be pulled up to VDDIO for compatibility with  
 future processors \*  
 Translation may be needed to meet the input requirements  
 of the regulator inputs (See datasheet for processor Voh  
 specs & regulator datasheet for Vih min requirements)

6-bit VID Implementation:  
 VID5:0 directly connects to VID5:0 of regulator.  
 VID1 should be pulled up to VDDIO for compatibility with future processors  
 NOTE: There is an incompatibility between the 5-bit VID code & 6-bit VID code x11111b. VID code 11111b is 0xFF for 5-bit VID controllers & a valid VID code for 6-bit VID controllers (011111b is 757mV & 111111b is 375mV). These are not planned to be operating VID<sub>tr</sub> for non-mobile processors so no adverse system implications will occur using a 5-bit VID or 6-bit controller in non-mobile implementations. Please see AMD Socket M2 Motherboard Design Guide, PID #33165 for more details.



These signals must be driven low during S3 and S5 states, including state transitions, to meet HT I/O Link Specification



## Erratum 133, Revision Guide for AMD NPT 0Fh Processors

## Erratum 133, Revision Guide for AMD NPT 0Fh Processors

CPU\_M\_VREF\_SUS

Layout: Place near CPU socket



**FOXCONN PCEG**

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# Processor Power & Ground

<http://www.bufanxiu.com>

VLD<sub>T</sub>\_RUN\_B is connected to the VLD<sub>T</sub>\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

## Bottomside Decoupling

Decoupling Between Processor and DIMMs  
Place as close to processor as possible.

Decoupling Between Processor and DIMMs

Place near processor on VLD<sub>T</sub> pour.

<b>FOXCONN</b>		
<b>FOXCONN PCEG</b>		
File		
<b>M2- 4 Power</b>		
Size	Document Number	Rev
C	<b>K8M890M01</b>	A
Date:	Friday, August 04, 2006	Sheet 11 of 32

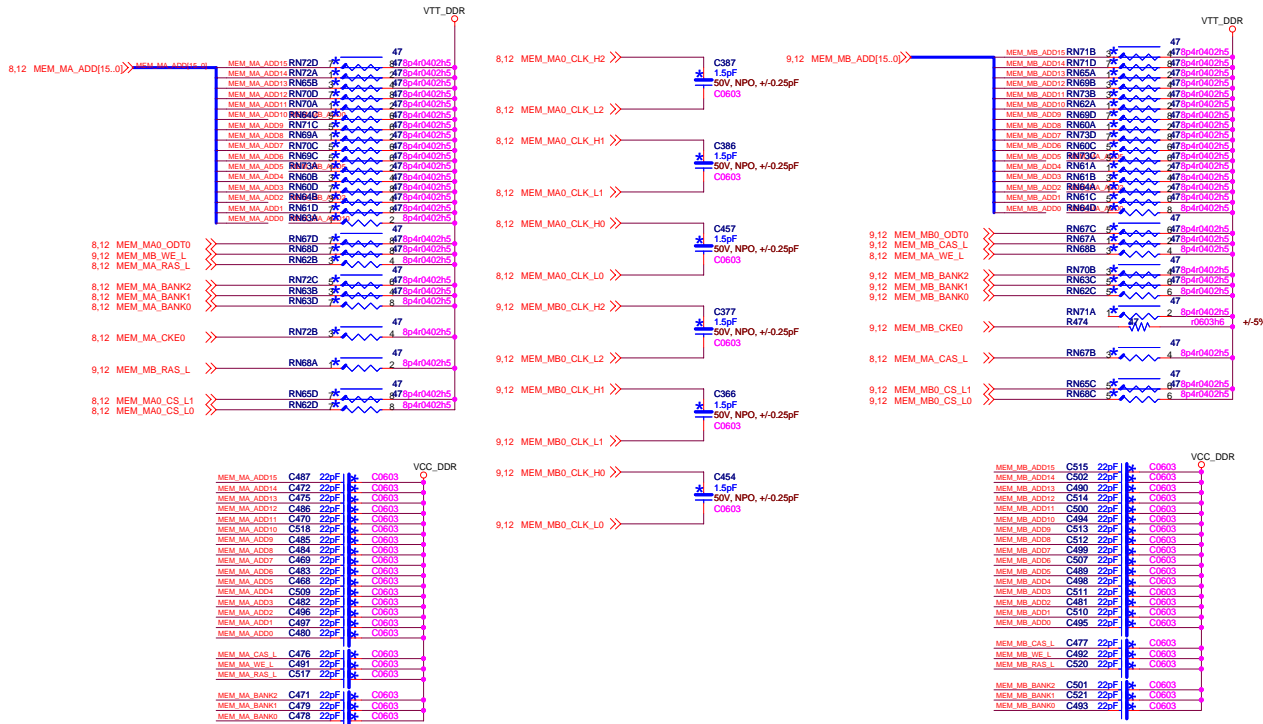
## DIMMB0



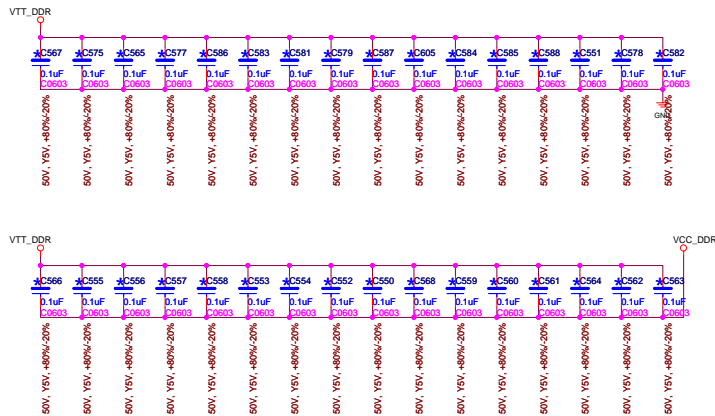
240

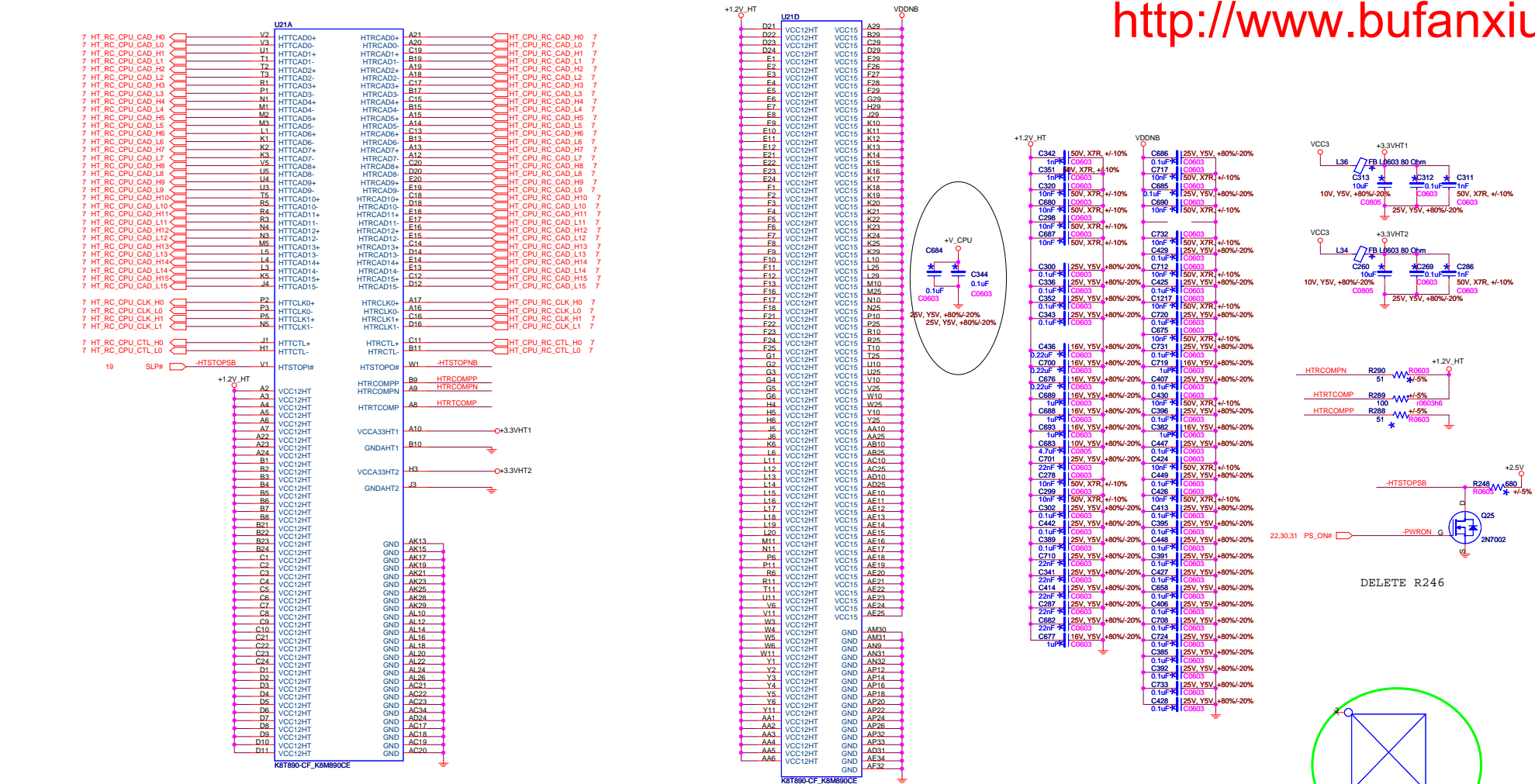


Title			
DDR SDRAM DIMM 1 - 2			
Size	Document Number		Rev
C	K8M890M01		A
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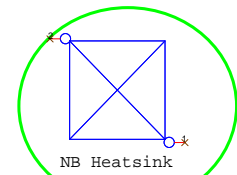
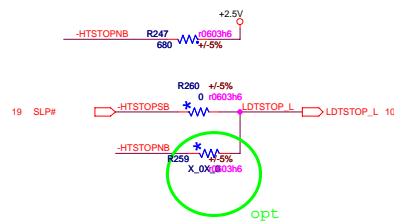


Layout: Spread out on VTT pour

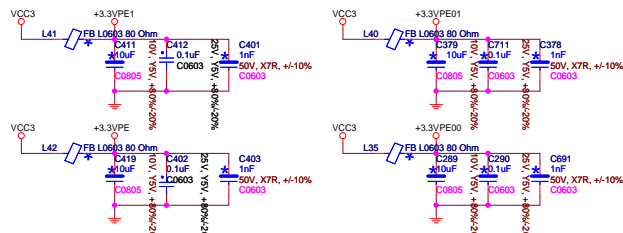
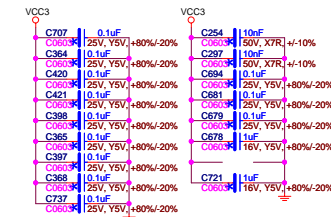
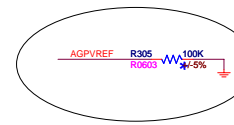
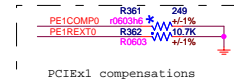
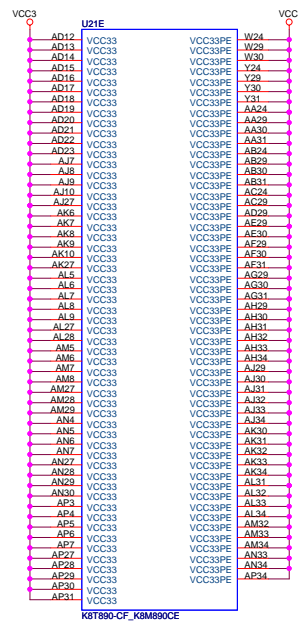




7 HT\_RC\_CPU\_CAD\_H[15..0] HT\_RC\_CPU\_CAD\_H[15..0]  
 7 HT\_RC\_CPU\_CAD\_L[15..0] HT\_RC\_CPU\_CAD\_L[15..0]  
 7 HT\_CPU\_RC\_CAD\_H[15..0] HT\_CPU\_RC\_CAD\_H[15..0]  
 7 HT\_CPU\_RC\_CAD\_L[15..0] HT\_CPU\_RC\_CAD\_L[15..0]





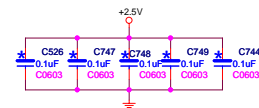




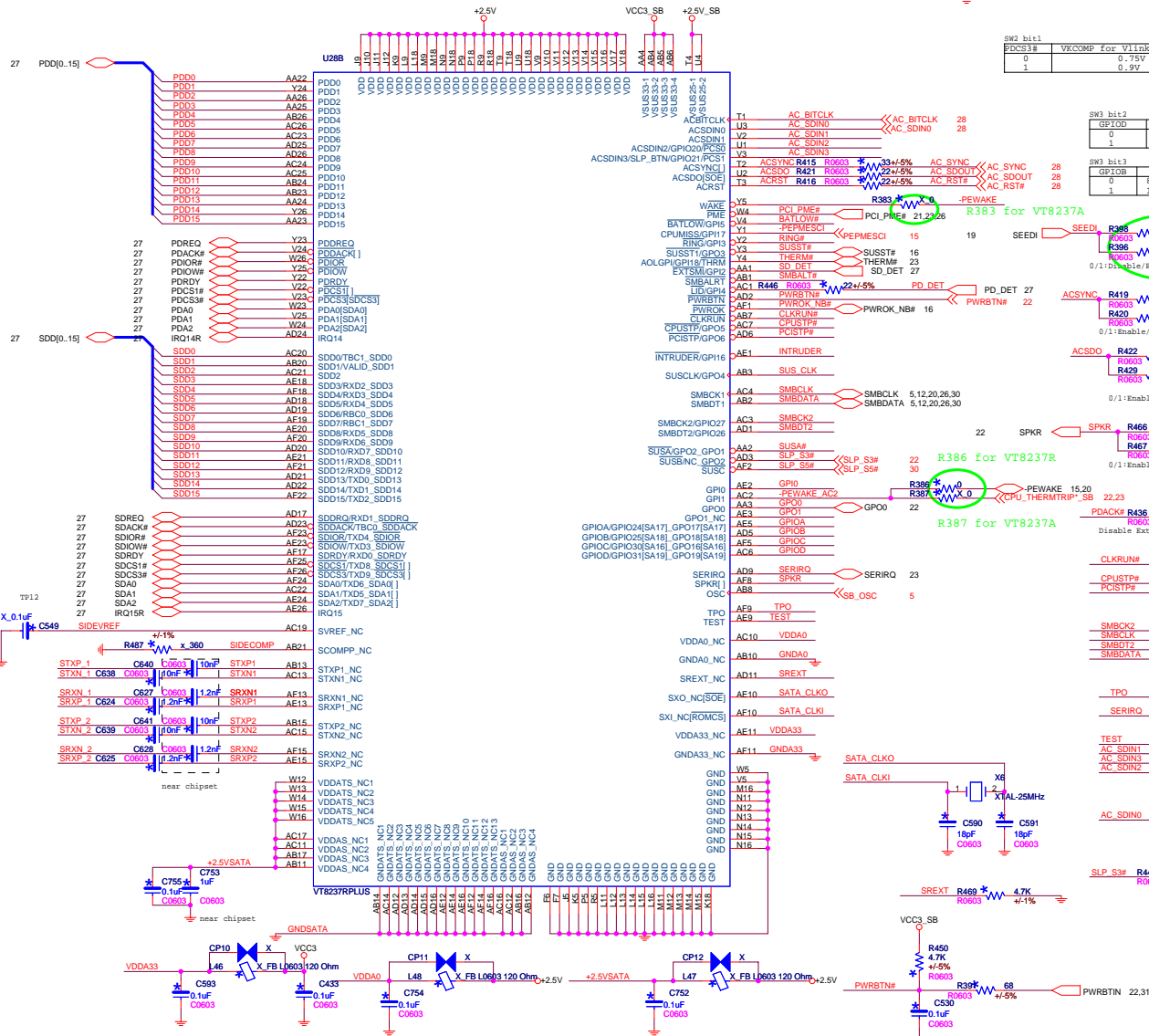
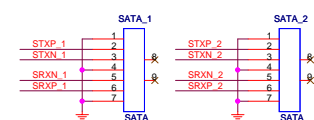
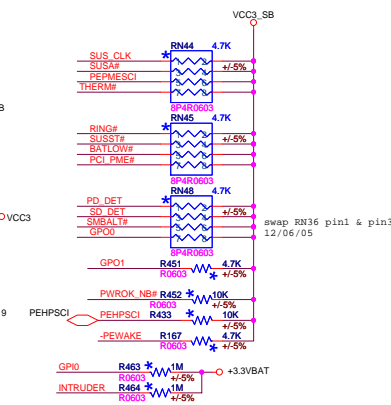
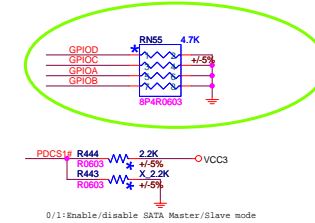
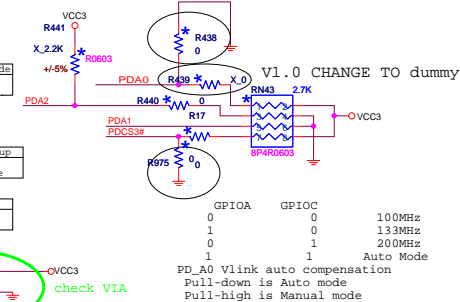


Rev

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change from 0 ohm to 2.7k ohm



PDCS#	VKCOMP for Vlink at 4X mode
0	0.75V
1	0.9V

GPIOD	GTL pullup
0	Enable
1	Disable

SW3 bit3	
GPIOB	IOQ Depth
0	8 Level
1	1 Level

SEEDI  SEEDI R398 4.7K  
R0603 +/-5%  
R396 X 4.7K  
R0603 +/-5%

PD\_DET 27  
BTN# 22

ACSYNC R419 4.7K  
R0603 \* +/-5%  
R420 X 4.7K

ACSDO R422 4.7K  
R0603 +/-5%  
R429 X 4.7K

0/1:Enable/disable auto

SPKR 

or VT8237R

or VT8237A

CPUSTP#

PCISTP#

8P4R0W0

[illegible]

TPO R468  
SERIRQ R0603 R465 R0603

AC\_SDINO R423 R0603

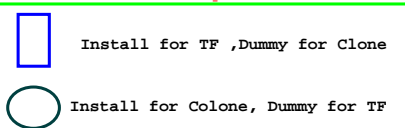
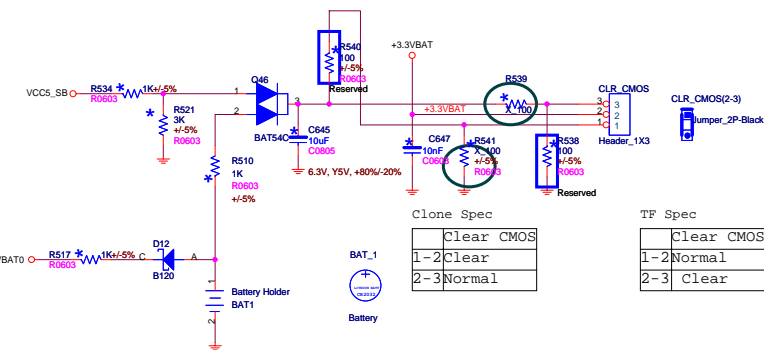
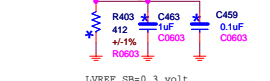
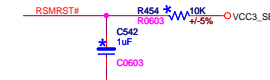
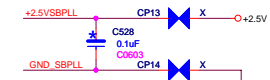
SLP S3# R449 X 4  
R0603 +/5%

68  
+/-5% PWRBTIN 22,31

	D
--	---

YTR237 R-PIPs Rev. CD	YTR237A Rev. CD	South Bridge	Function
SDOUT	SDOUT	Auto Reboot 0:1: Enable/Disable	For default setting, it is disable
SEEDIN	SEEDIN	Eliminate LAN T12PROM SDCN: 0:1: Enable/Disable SEEDIN: 1:0: Enable/Disable	For default setting, it is disable
SPKR	SPKR	CPU Frequency Stepping 0:1: Enable/Disable	For default setting, it is disable
ACYNIC	ACYNIC	LPC FWH Command 0:1: Enable/Disable	For default setting, it is disable
PDCSI	N/A	SATA Master Slave Mode 0:1: Master Slave mode/Master Master mode Set 2, where master/master/PIV	
FDCKAC	N/A	Control SATA PIV 0:1: Enable/Disable	
N/A	N/A	Integrated LAN Reset method 1: For Desktop	

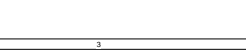
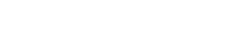
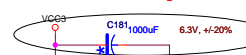
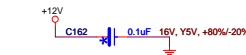
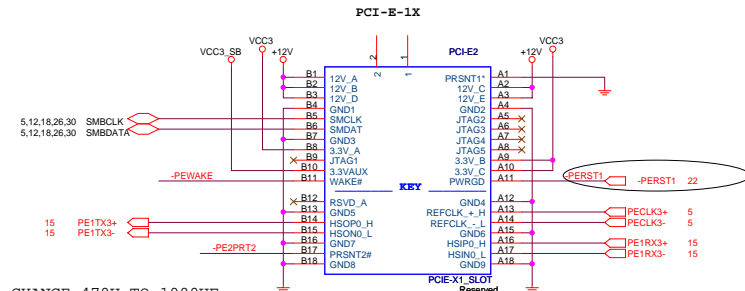
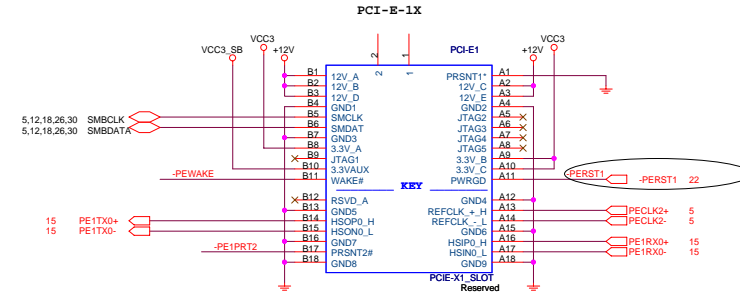
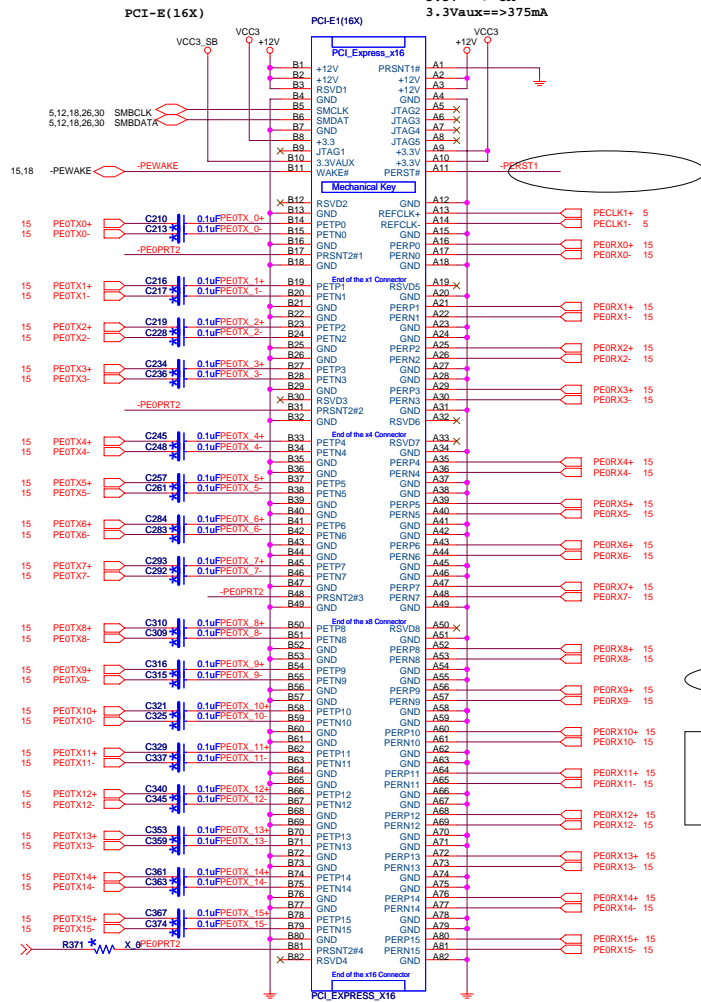
\* For Notebook  
 (Without Wake On LAN feature from SATA)



# Connector combine R.M.

J8,J9: 1-2 short (PORT 31)  
2-3 short (PORT 25)

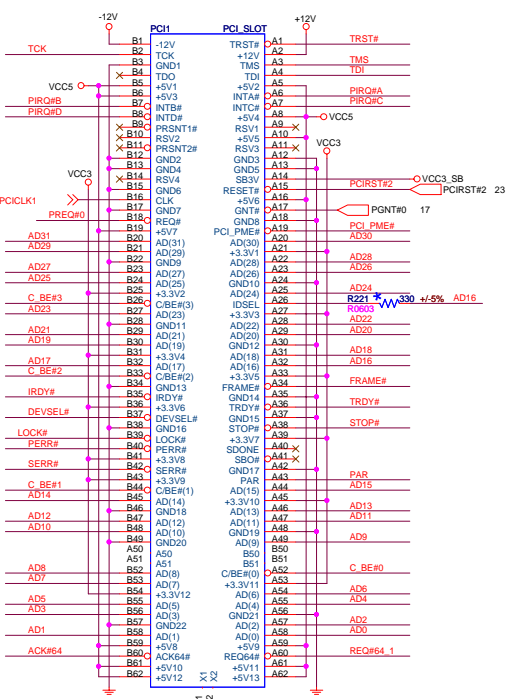
12V ==> 5.5A for x16 slot ,75 Watt  
3.3V==> 3A  
3.3Vaux==>375ma



C181 CHANGE 470U TO 1000UF

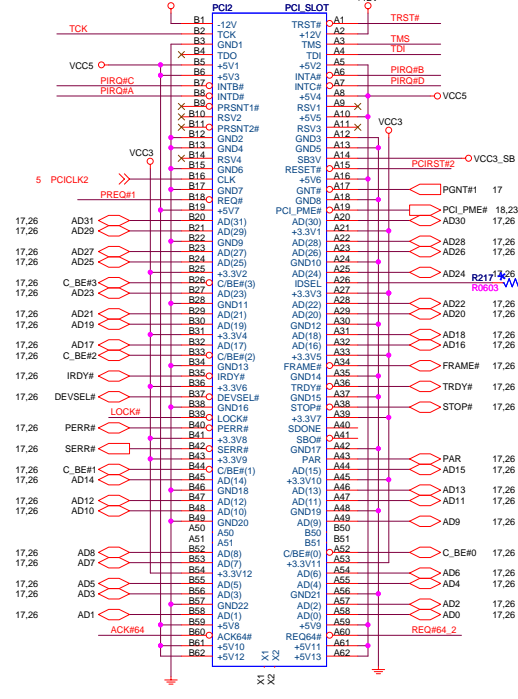
The system board designer determines the pull-up voltage

## PCI SLOT 1



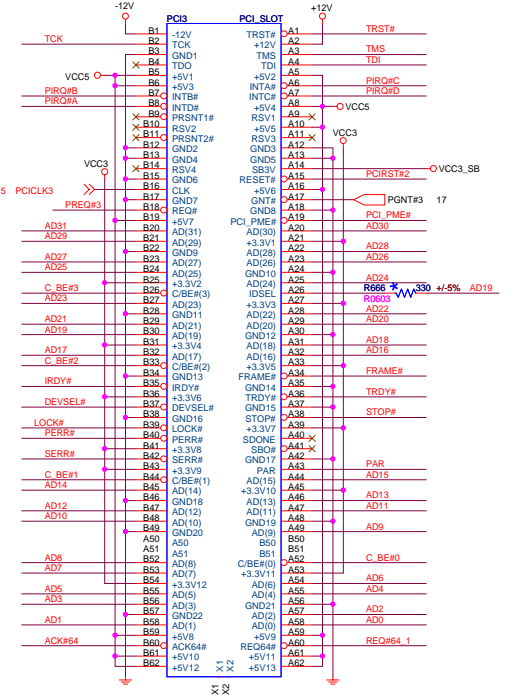
ISDEL = AD16  
MASTER = PREQ#0  
PIRQ#A

## PCI SLOT 2



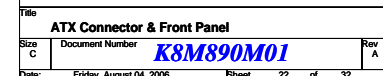
ISDEL = AD17  
MASTER = PREQ#1  
PIRQ#B

## PCI SLOT 3

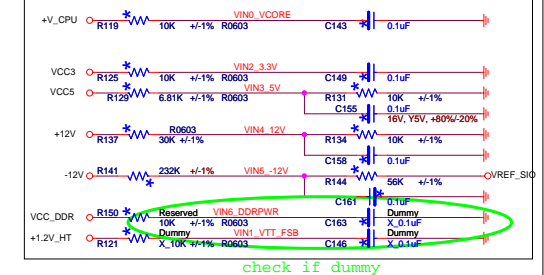
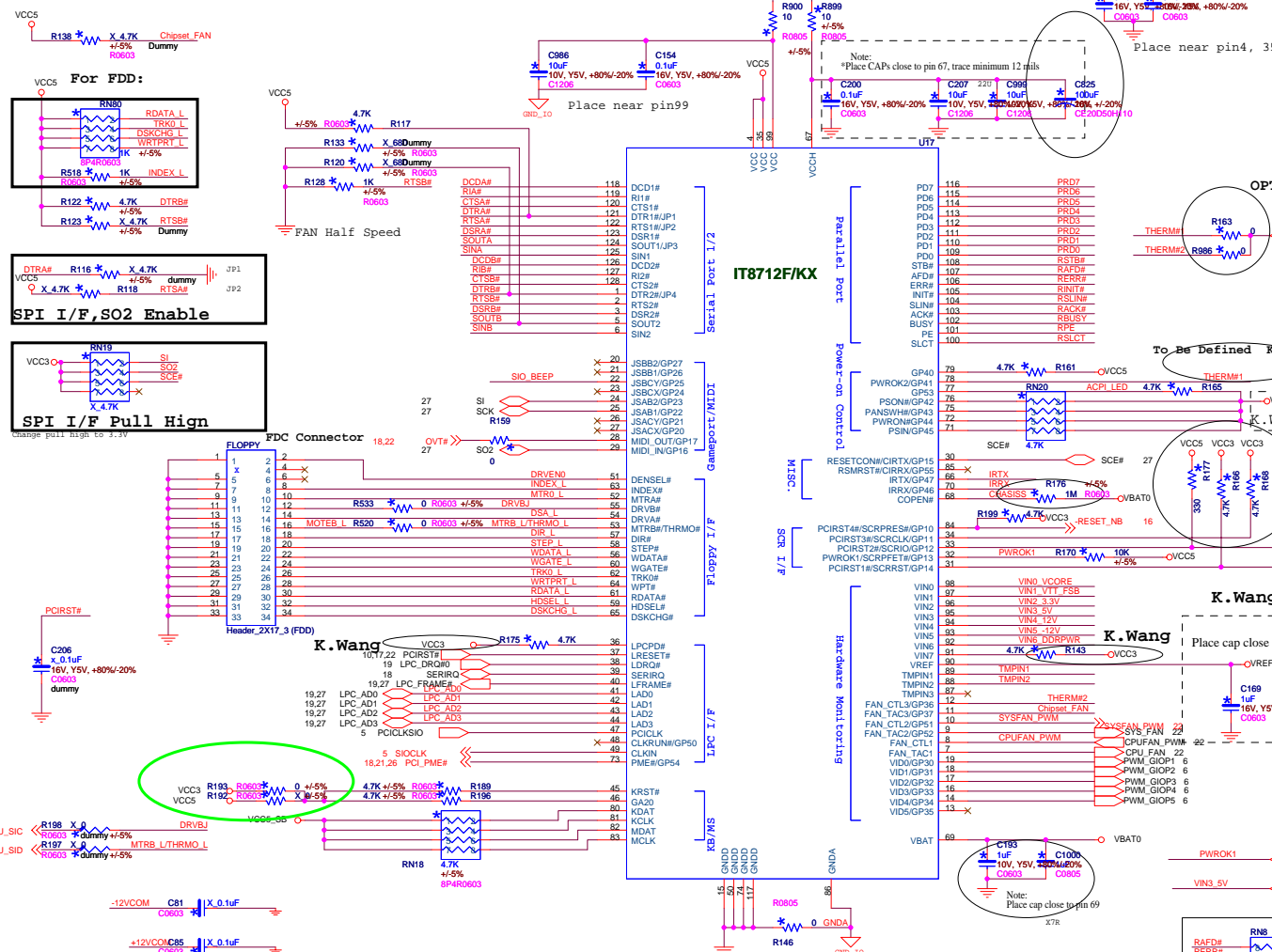




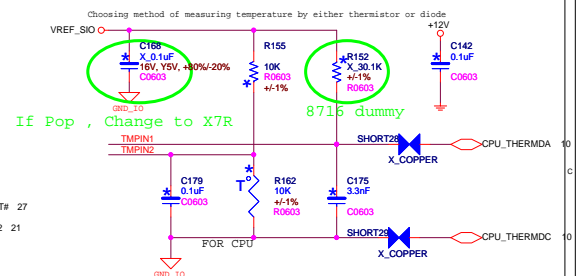
```
New FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
```



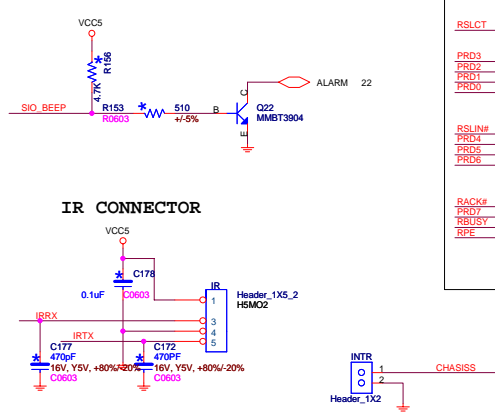
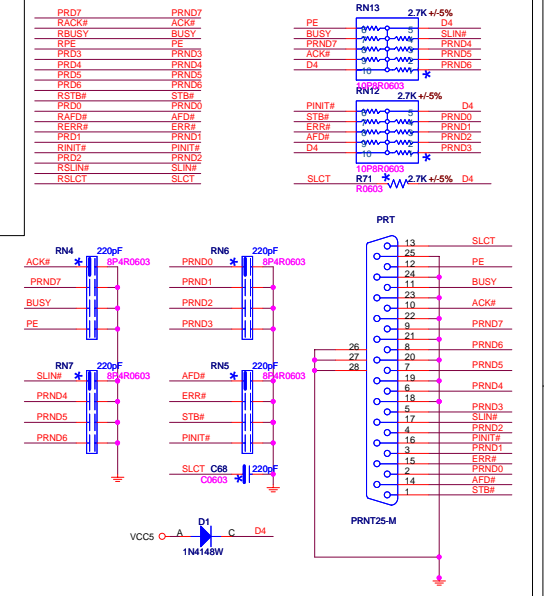




## Temperature Monitor




## Print Port



**FOXCONN PCEG**

Title			
SIO IT8716_AX/BX			
Size	Document Number		Rev
C	K8M890M01		A
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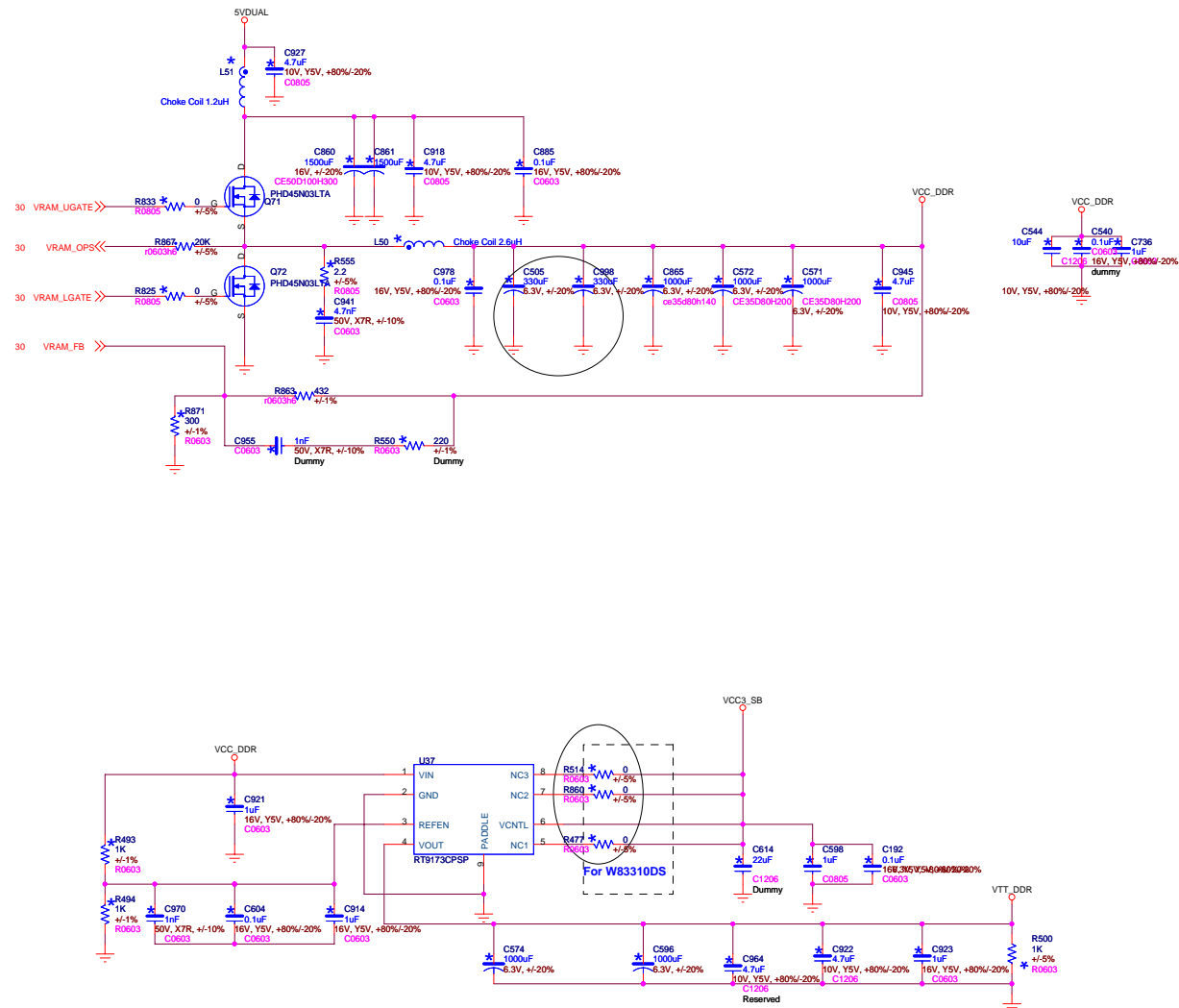


**FOXCONN PCEG**

Title		
VGA Connector		
Size	Document Number	Rev
C	<b>K8M890M01</b>	A
Date:	Friday, August 04, 2006	Sheet 24 of 32

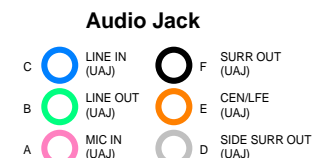
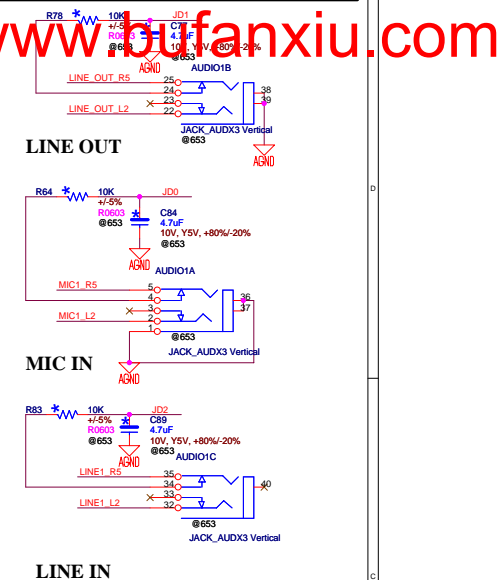
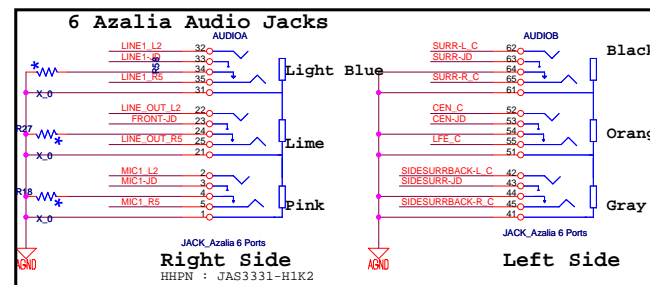
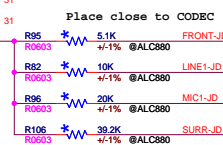
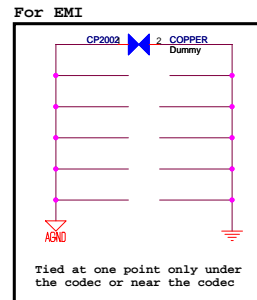
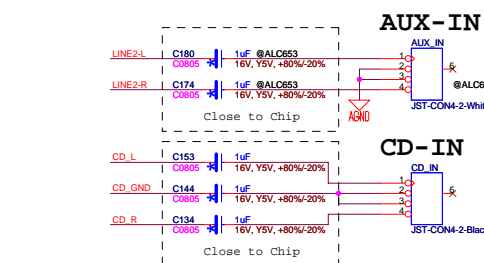
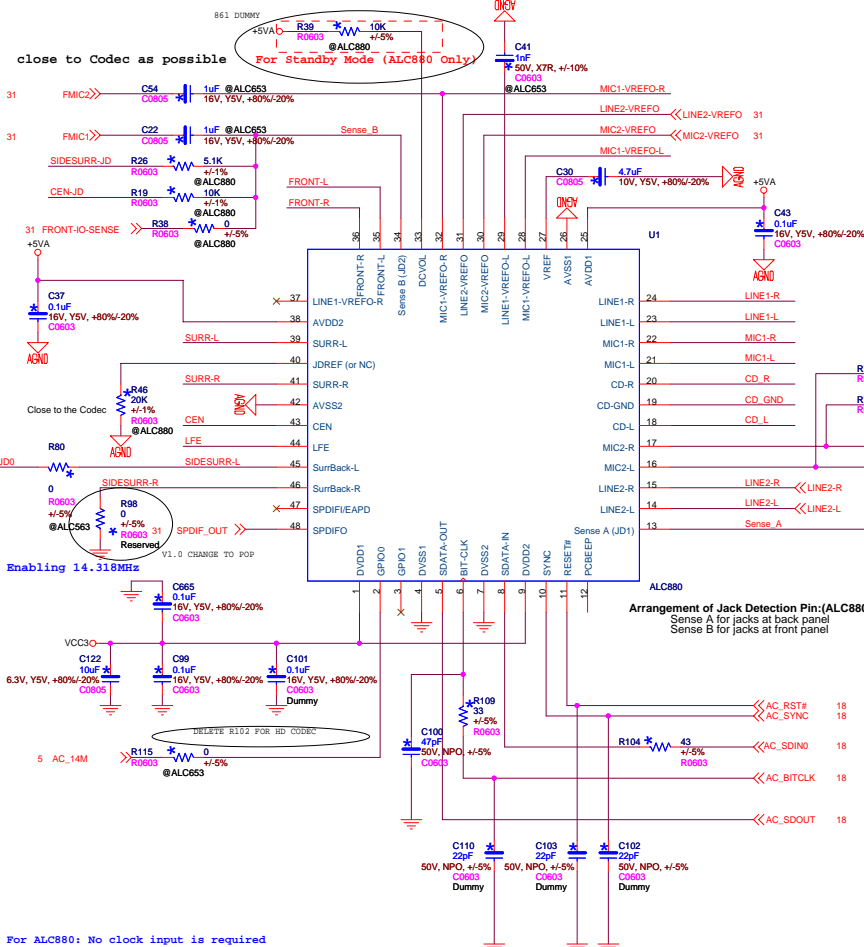


```
Did not support S3
wake-up
```

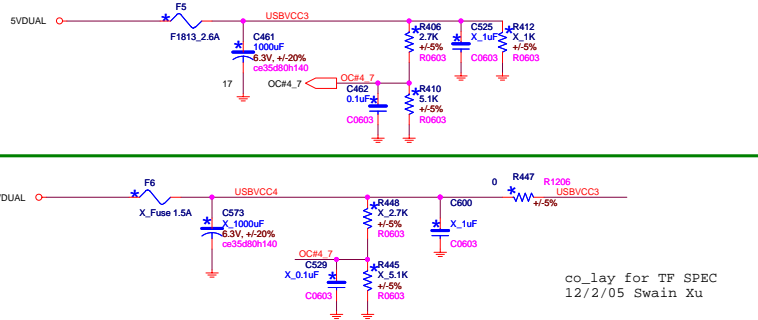




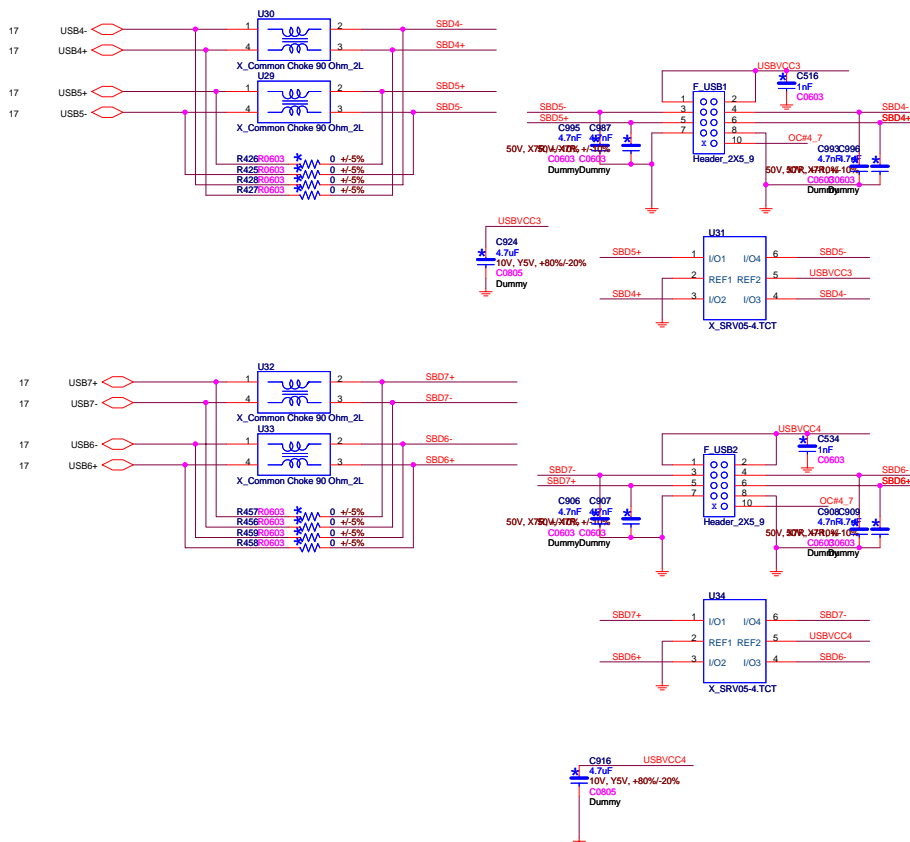




# POWER CIRCUIT FOR USB PORT 4,5,6,7

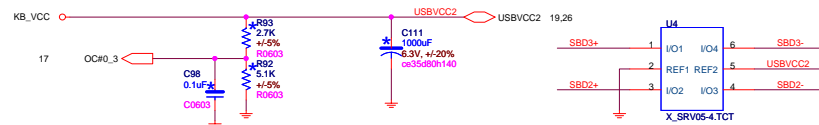


# FRONT PANEL USB CONNECTOR FOR USB PORT 4,5,6,7

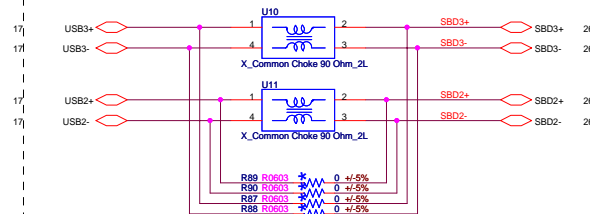


# POWER CIRCUIT FOR USB PORT 0,1,2,3

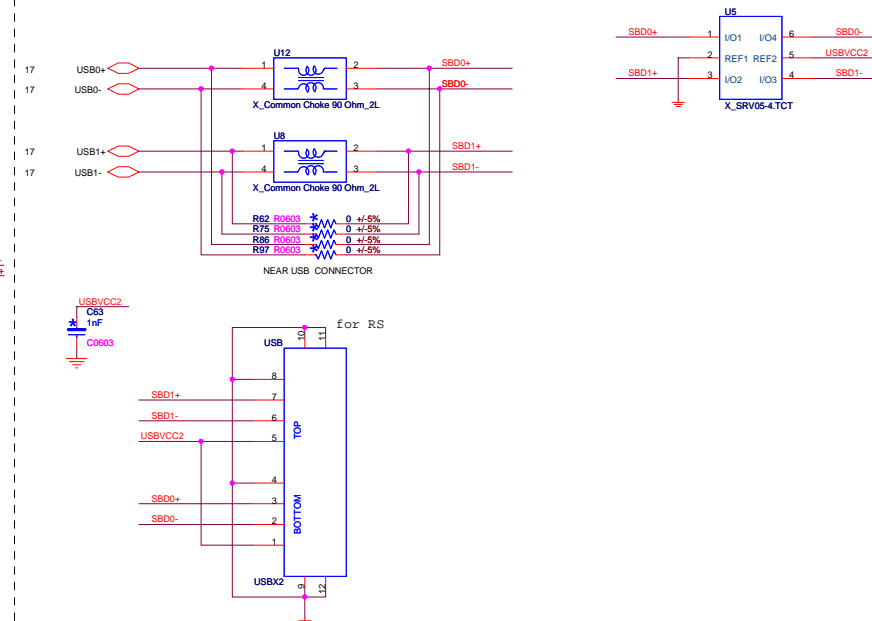
<http://www.bufanxiu.com>



# REAR PANEL USB CONNECTOR FOR USB PORT 2,3



# REAR PANEL USB CONNECTOR FOR USB PORT 0,1



Add 10 pcs cap (dummy)





6.DUMMY PART  
CHECK WITH THOMAS BOM

CHECK OVER CPU VOLTAGE BOM VALUE:R300,R301,R302,R303,R304

CHECK CHANGE REASON:C688,C689,C693,C718,C753,C736

CHECK FAB A DUMMY PART  
CHECK V1.0 DUMMY PART

CHANGE EMI SOLUTION TO BOM ,,CHANGE SI BUG TO BOM

Change List		
Title		
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